

1. A semiconductor device of a memory cell array of aligning plural numbers of semiconductor memory element in a matrix-like manner, said element comprising:

a drain region;

a gate electrode made of either one of metal and semiconductor, for controlling potential of said channel region;
and

a first semiconductor memory cell and a second semiconductor memory cell neighboring with each other share said source region in common.

a source region;

a channel region of semiconductor connecting between said source region and said drain region;

a gate electrode made of either one of metal and semiconductor, for controlling potential of said channel region; and

plural numbers of charge storage regions formed in vicinity of said channel, wherein:

a first semiconductor memory cell and a second semiconductor memory cell neighboring with each other share said source region in common; and

said second semiconductor cell shares said drain region in common with a third semiconductor memory cell neighboring therewith.

3. A semiconductor device of a memory cell array of aligning plural numbers of semiconductor memory element in a matrix-like manner, said element comprising:

a source region;

a drain region;

a channel region of semiconductor connecting between said source region and said drain region;

a gate electrode made of either one of metal and semiconductor, for controlling potential of said channel region; and

plural numbers of charge storage regions formed in vicinity of said channel, wherein:

a layout of cell separation regions of said memory cell array is in a rectangular shape, aligning them in parallel to each other, substantially;

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a layout of word lines for connecting said gate electrodes of said semiconductor memory cells is in a rectangular shape, aligning them in parallel to each other, substantially;

said semiconductor memory cell has such structure that it shares a diffusion region of said source region in common with only one (1) cell neighboring therewith;

said source lines of at least three (3) of said semiconductor memory cells are connected with one another through either one of diffusion layer wiring and metal wiring; and

said rectangular cell separation regions of aligning in parallel to each other and said rectangular diffusion layers of aligning in parallel to each other are in parallel to each other, substantially, and said rectangular cell separation region of aligning in parallel to each other and said word lines aligning in parallel to each other are perpendicular to each other in a positional relationship therebetween.

4. A semiconductor device of a memory cell array of aligning plural numbers of semiconductor memory element in a matrix-like manner, said element comprising:

a source region;

a drain region;

a channel region of semiconductor connecting between said source region and said drain region;

a gate electrode made of either one of metal and semiconductor, for controlling potential of said channel region; and

plural numbers of charge storage regions formed in vicinity

of said channel, wherein:

a layout of cell separation regions of said memory cell array is in a rectangular shape, aligning them in parallel to each other, substantially;

a layout of word lines for connecting said gate electrodes of said semiconductor memory cells is in a rectangular shape, aligning them in parallel to each other, substantially;

said semiconductor memory cells have such structure that plural number of said source regions thereof are connected with each other through the diffusion layers;

a layout of the diffusion layers connecting the plural numbers of said source regions is in a rectangular shape, aligning them in parallel to each other, substantially; and

said rectangular cell separation regions of aligning in parallel to each other and said rectangular diffusion layers of aligning in parallel to each other are in parallel to each other, substantially, and said rectangular cell separation region of aligning in parallel to each other and said word lines aligning in parallel to each other are perpendicular to each other in a positional relationship therebetween.

5. A semiconductor memory cell, comprising:

a channel region made of semiconductor;

plural numbers of charge storage regions in vicinity of said channel region;

a first gate electrode made of either one of metal and semiconductor for controlling potential of said plural numbers of said charge storage regions; and

a second gate electrode made of either one of metal and semiconductor for controlling potential of portions other than said channel region on a semiconductor surface.

6. A semiconductor memory cell, comprising:

a channel region made of semiconductor;

a channel region made of semiconductor, connecting between said source region and said drain region;

plural numbers of charge storage regions in vicinity of said channel region;

a first gate electrode made of either one of metal and semiconductor for controlling potential of one portion of said channel region and the plural numbers of said charge storage regions; and

a second gate electrode made of either one of metal and semiconductor for controlling potential of portions of the channel region other than that one portion of said channel region.

7. A semiconductor memory cell, comprising:

a source region;

a drain region;

a channel region of semiconductor connecting between said source region and said drain region;

plural numbers of charge storage regions in vicinity of said channel region;

sidewall structures made of either one of semiconductor

and metal, provided at both sides of said gate region; and

an insulation film formed between said sidewall structures and said gate electrode.

8. A semiconductor memory cell, as defined in the claim 7, wherein:

one of said sidewall structures at both sides of said gate electrode, being near to the source region, is connected with said source region; and

the other, being near to the drain region, is connected with said drain region.

9. A semiconductor memory cell, as defined in the claim 8, wherein:

said sidewall structures and either one of the source region and the drain region are connected through either one of semiconductor or metal, which is selectively piled up on said sidewall structures and either one of the source region and the drain region.

10. A semiconductor memory cell in a memory cell array, comprising:

the semiconductor memory cells as defined in either one of the claims 5 to 9, being aligned in plural numbers thereof, wherein they are driven by a data line and a word line, wherein:

drain regions of plural numbers of semiconductor memory cells are connected to a same data line;

second gates of said plural numbers of said semiconductor memory cells, which are connected to the same data line at said

drain regions thereof, are connected with each other; and

first gates of said plural numbers of said semiconductor memory cells, which are connected to the same data line at said drain regions thereof, are connected with word lines, being different from each other.

11. A semiconductor device of a memory cell array, aligning semiconductor memory cells as defined in the claim 5, in plural numbers thereof, comprising:

a first semiconductor memory cell and a second semiconductor memory cell are connected, so that channel currents thereof flow in series;

on one of both sides of a first gate electrode of said first semiconductor memory cell, opposite to a second gate electrode of said first semiconductor memory cell, is disposed a second gate electrode of said second semiconductor memory cell.

12. A semiconductor memory device, comprising:

a channel region made of semiconductor;

plural numbers of charge storage regions in vicinity of said channel region;

a first gate electrode made of either one of metal and semiconductor for controlling potential of said channel region and said plural numbers of charge storage regions;

a second gate electrode made of either one of metal and semiconductor for controlling potential of a portion adjacent to said channel region on a semiconductor surface; and

a third gate electrode made of either one of metal and

semiconductor, being formed adjacent to said channel region on the semiconductor surface, for controlling potential of a portion on an opposite side of said second gate electrode.

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